(TRANSLATION)

Reference No.:PH19033 Mailing No.:016286
Mailing Date: January 22, 2008

NOTICE OF GROUND FOR REJECTION

Re: Patent Application No.2007-107561
Drafting Date: January 11, 2008
From: TOYOSHIMA, Hiromi, Examiner of Patent Office 9426 3S00
To: Junzo OGAWA, Representative for Applicant of Patent (and one other)
Applied clauses: Sections 29 (2) and 39

This application is deemed to be rejected on the following grounds. If the applicant has any objection against this, an argument must be filed within 60 days.

GROUND

(Ground 1)

The inventions relating to the following claims of this application are found to be easily invented by the person of ordinary knowledge in the art, based on the inventions disclosed in the paper publications distributed in Japan or in the foreign countries prior to the filing date of this application, and the present application cannot be allowed by virtue of the provisions of Sec.29 (2) of Patent Law:

(Ground 2)

The inventions relating to the following claims of this application are found to be the same as the application filed on the same day as this application was filed on and the present application cannot be allowed by virtue of the provisions of Sec. 39 (2) of Patent Law if the notification has not been made by the applicant as described by the order letter issued in the name of Commissioner of Patents on the same mailing date of this notice.

REMARKS

1. As to Ground 1

- Claim 1
- Reference 1
- Remarks: The Reference 1 discloses in a multilayer printed wiring board wherein the interlaminar insulating layer is formed by covering a substrate with an

internal layer of conductor circuit formed thereon and an outer-layer of the conductor circuit is formed on the interlaminar insulating layer, the multilayer printed wiring board has a roughened layer formed on the surface of the interlaminar insulating layer, and the outer-layer of the conductor circuit comprising of an electroless plating film adhered to the roughened layer and an electrolytic plating film formed on the electroless plating film.

- Claims 2 and 3
- References 1 and 2
- Remarks: The Reference 2 discloses that the same kind of a roughened layer is formed on an upper face of an interlaminer insulating layer and on a surface of an internal wall of openings for forming via-holes by the same roughening treatment.

- Claims 4 and 5
- References 1-3
- Remarks: The Reference 3 discloses that in a multilayer printed wiring board wherein an outermost layer of a conductor circuit which solders should be supplied to is formed on an interlaminer insulating layer positioned as an outermost layer among interlaminer insulating layers, a solder resist layer having openings though which a surface of the conductor layer is partially exposed is formed on the outermost layer of the conductor circuit and the peripheral part of the conductor circuit is covered by the solder resist layer.

- Claim 6
- References 1 and 4
- Remarks: The Reference 4 discloses the method wherein an electroless plating film is formed, a plating resist is formed on the electroless plating film, an electrolytic plating film is formed by electrolytic plating treatment on the parts of the electroless plating film where the plating resist is not formed, after the plating resist is removed, the electroless plating film under the plating resist is removed by dissolving with the etching treatment, and an outermost layer of the conductor circuit comprising of the electroless plating film and the electrolytic plating film is thus formed.

- Claims 7 and 8
- References 1, 2 and 4
- Remarks: The Reference 2 discloses the method of forming the same kind of roughened layer on an upper face of an interlaminer insulating layer and on a surface of an internal wall of openings for forming via-holes by the same kind of roughening treatment.

2. As to Ground 2

- Claims 2,3,7 and 8
- Reference 5
- Remarks: The Reference 5 discloses a multilayer printed wiring board and a method of producing the same.

REMARKS (Please refer to the list of references)

1. JP-A-8-181438
2. JP-A-3-3297
3. JP-A-8-242064
4. JP-A-5-304362
5. Japanese Application No. of 2002-227202 (Laid-open No. of JP 2003-60342)

RECORD OF SEARCH RESULT FOR PRIOR ART REFERENCES

- Genre in which a search was conducted: IPC, H05K1/00-3/46

This record of search result for prior art references does not constitute grounds for rejection.

Inquire about the contents of this Notice of Ground for Rejection to:
TOYOSHIMA, Toshimi
Division for Transporting and Setting-Up (Setting-Up and Manufacturing) in Second Department of Patent Examination
Telephone No.: 03(3581)1101 (x3389)